

WHAT IS CLAIMED IS:

1. A computer system comprising:
 - a first processor configured to cause an operating system to be booted;
 - a test module;
 - a component coupled to the test module; and
 - a power supply coupled to the test module and the component;wherein the test module is configured to cause a first signal to be provided to the power supply to cause a first voltage to be provided to the component, and wherein the test module is configured to cause a first test to be performed on the component subsequent to the first voltage being provided to the component and the operating system being booted.
2. The computer system of claim 1 wherein the test module is configured to cause a second signal to be provided to the power supply to cause a second voltage to be provided to the component, and wherein the test module is configured to cause a second test to be performed on the component subsequent to the second voltage being provided to the component and the operating system being booted.
3. The computer system of claim 2 wherein the component is configured to operate at a third voltage, wherein the first voltage is greater than the third voltage, and wherein the second voltage is less than the third voltage.
4. The computer system of claim 3 wherein the first voltage is approximately 10% greater than the third voltage, and wherein the second voltage is approximately 10% less than the third voltage.
5. The computer system of claim 1 wherein the test module is configured to provide a second signal to the operating system to cause the component to be deallocated from use by the operating system.

6. The computer system of claim 5 wherein the operating system is configured to provide a third signal to the test module in response to causing the component to be de-allocated from use by the operating system.
7. The computer system of claim 1 wherein the test module is configured to detect an error in the component in response to the first test being performed, and wherein the test module is configured to cause remedial action associated with the component to be performed in response to detecting the error.
8. The computer system of claim 1 wherein component comprises a second processor.
9. The computer system of claim 1 wherein component comprises an input / output (I/O) device.
10. The computer system of claim 1 further comprising:
an input / output (I/O) controller coupled to the component;
wherein the test module is coupled to the I/O controller.
11. The computer system of claim 10 wherein the I/O controller comprises an I2C controller.
12. A method performed by a test module in a computer system comprising:
causing a first component to be de-allocated from use by an operating system;
causing a first voltage to be applied to the first component;
performing a first test on the first component; and
notifying the operating system in response to detecting a first error in performing the test.
13. The method of claim 12 further comprising:

causing a second voltage that differs from the first voltage to be applied to the first component;

performing a second test on the first component; and

notifying the operating system in response to detecting a second error in performing the second test.

14. The method of claim 12 further comprising:

causing the first component to be re-allocated to use by the operating system subsequent to performing the first test.

15. The method of claim 12 further comprising:

reporting results of the first test to the operating system.

16. The method of claim 12 further comprising:

allocating a second component for use by the operating system in response to de-allocating the first component from use by the operating system.

17. A computer system comprising:

a processor configured to cause an operating system to be booted;

a component;

a power supply coupled to the component;

a first means for providing a first signal to be provided to the power supply to cause a first voltage to be provided to the component; and

a second means for causing a first test to be performed on the component subsequent to the first voltage being provided to the component and the operating system being booted.

18. The computer system of claim 17 wherein the first means is for providing a second signal to the power supply to cause a second voltage to be provided to the component, and wherein the second means is for causing a second test to be performed on the component subsequent to the second voltage being provided to the component and the operating system being booted.

19. The computer system of claim 17 wherein the second means is for providing a second signal to the operating system to cause the component to be de-allocated from use by the operating system.

20. The computer system of claim 17 wherein the second means is for detecting an error in the component in response to the first test being performed, and wherein the second means for causing remedial action associated with the component to be performed in response to detecting the error.